Universidade de São Paulo - São Carlos,SP
Instituto de Ciências Matemáticas e de Computação

USP - ICMC - SSC
SSC 0510 - Informática - 2o. Semestre 2009

Disciplina de Arquitetura de Computadores

Prof. Fernando Santos Osório
Email: fosorio [at] { icmc. usp. br , gmail. com }
Página Pessoal: http://www.icmc.usp.br/~fosorio/

Estagiário PAE Maurício Dias - Email: acdias29 [at] yahoo.com.br

Material on-line: COTEIA - http://coteia.icmc.usp.br

Aula 07

Aula 07 – Microprocessadores

Conteúdos Abordados:

1. **Microprocessador 6502**
2. **Microprocessador Intel 8080, 8085**
3. **Microprocessador Zilog Z80**
4. **Família Motorola 68000**
5. **Microprocessador Intel 8086**
6. **Família de Microprocessadores Intel 80x86:**
   8086, 286, 386, 486, 486DX, 586 (Pentium)
   MMX, Celeron, Centrino, ...

1. Microprocessador 6502

Arquitetura 6502

Microprocessador de 8 bits dados e 16 bits de endereço

Registers

The 6502 only has 6 registers. Five are 8 bits wide, one is 16 bits wide.

	A	Accumulator
	X	Index Register X
	Y	Index Register Y
PCH	PCL	Program Counter
	S	Stack Pointer
	P	Processor Status (Flags)

Processor Status Register

N	V	-	B	D	I	Z	C

N - Negative Flag
V - Overflow Flag
B - Break Command
D - Decimal Mode
I - Int. Disable
Z - Zero Flag
C - Carry Flag

Accumulator **8 bits** **A**

* Refs:
Leventhal, Lance A. (1986). 6502 Assembly Language Programming 2nd Edition. Osborne/McGraw-Hill.
Leventhal, Lance A. (1982). 6502 Assembly Language Subroutines. Osborne/McGraw-Hill. ISBN 0931988594.

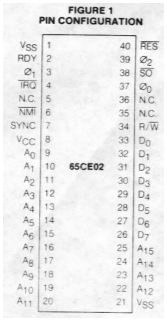
Microprocessador 6502

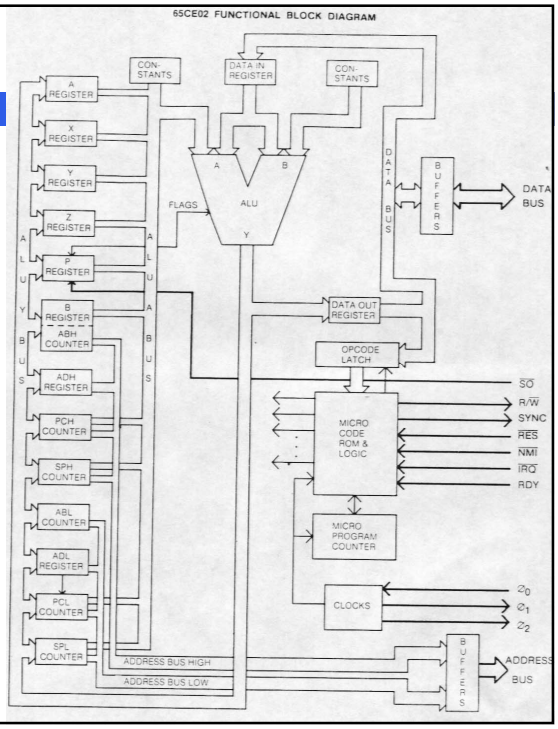
COMMODORE SEMICONDUCTOR GROUP
a division of Commodore Business Machines, Inc.

CMOS

65CE02 MICROPROCESSOR

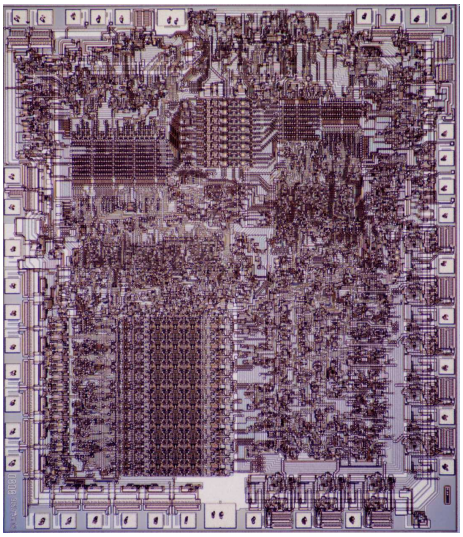
FIGURE 1
PIN CONFIGURATION

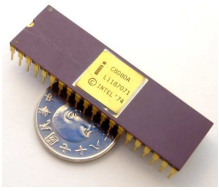




2. Microprocessador Intel 8080

Arquitetura Intel 8080

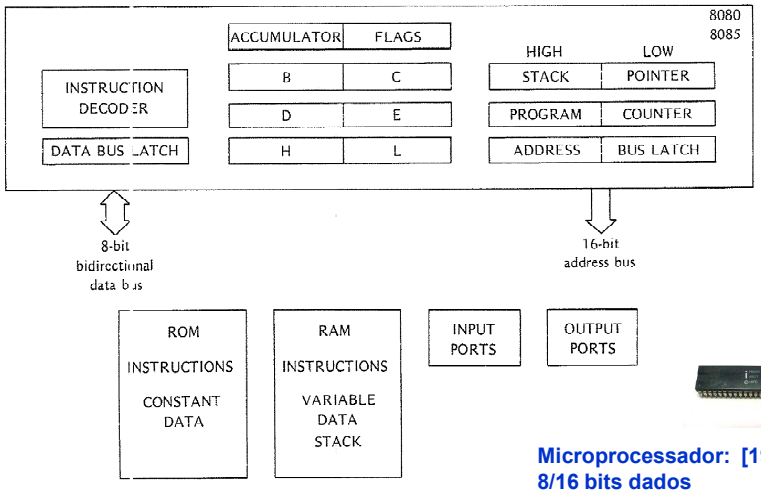




Microprocessador: [1974]
8/16 bits dados
16 bits de endereço

2. Microprocessador Intel 8080

Arquitetura Intel 8080



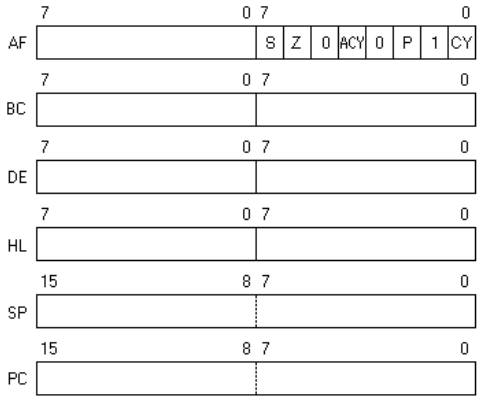
8080/8085 Internal Registers

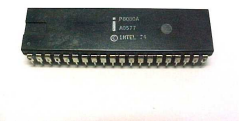
Microprocessador: [1974]
8/16 bits dados
16 bits de endereço

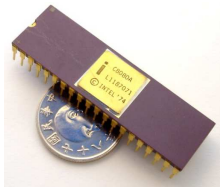
2. Microprocessador Intel 8080 / 8085

Arquitetura Intel 8080 / 8085

CPU Registers







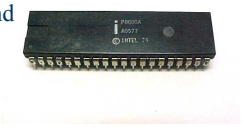
Microprocessador de 8/16 bits dados e 16 bits de endereço

2. Microprocessador Intel 8080 / 8085

Arquitetura Intel 8080 / 8085

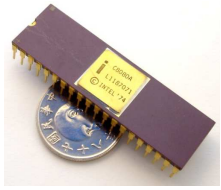
CPU Registers

"From a software point of view there is only a small difference between the 8080 and 8085. In fact the main difference is that the 8085 has 2 extra instructions to deal with its serial input and serial output pins and interrupt system.



Apart from that the 8085 uses less cycles to complete its instructions, making it faster than the 8080.

The hardware differences between the two processors are more spectacular. You'd better use a 8085 if you plan to use either of the 2 processors because it is much easier to interface with."

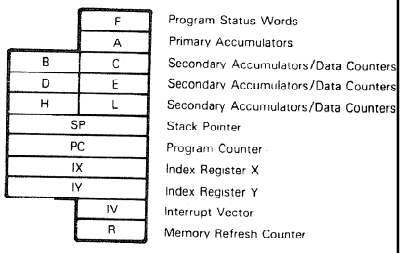


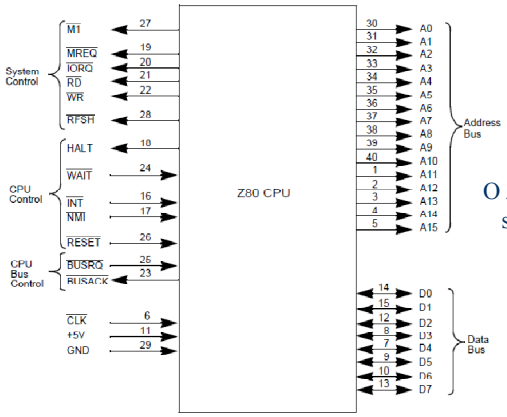
http://www.sbprojects.com/sbasm/8080.htm

Microprocessador de 8/16 bits dados e 16 bits de endereço

3. Microprocessador Z80

Arquitetura Zilog Z80





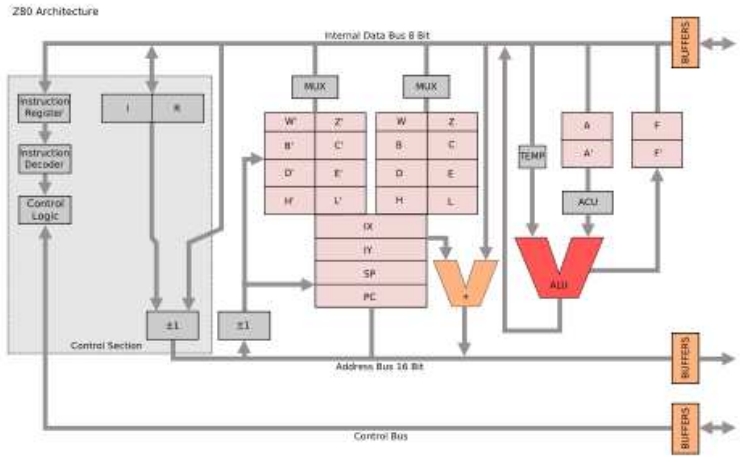
O Z80 foi desenvolvido para ser um substituto do 8080 com algumas Vantagens...

Microprocessador: [1976]
8/16 bits dados
16 bits de endereço

USP - SSC-510 - Informática T1 / 2009-2
Arquitetura de Computadores
Prof. Fernando Osório

3. Microprocessador Z80

Arquitetura Zilog Z80



3. Microprocessador Z80

Arquitetura Zilog Z80

CPU Registers

Main Registers Set

Accumulator	Flags
A	F
B	C
D	E
H	L

Alternative Registers Set

Accumulator	Flags
A'	F'
B'	C'
D'	E'
H'	L'

General Purpose Registers

Interrupt Vector I	Memory Refresh R
Index Register	IX
Index Register	IY
Stack Pointer	SP
Program Counter	PC

Special Purpose Registers

3. Microprocessador Z80

Arquitetura Zilog Z80

CPU Registers

Main Register Set / Alternate Register Set

Accumulator	Flags	Accumulator	Flags
A	F	A '	F '
B	C	B '	B '
D	E	D '	E '
H	L	H '	L '

General Purpose Registers

Interrupt Vector I	Memory Refresh R
Index Register	IX
Index Register	IY
Stack Pointer	SP
Program Counter	PC

Special Purpose Registers

8080 / 8085
X
Z80

Z80 CPU Register Configuration

3. Microprocessador Z80

Arquitetura Zilog Z80

The 8080 compatible registers:

AF - 8-bit accumulator (A) and flag bits (F)
Flags: Carry, Zero, Minus, Parity/overflow, Half-carry (used for BCD), and an Add/Subtract flag (usually called N) also for BCD

BC - 16-bit data/address register or two 8-bit registers
DE - 16-bit data/address register or two 8-bit registers
HL - 16-bit accumulator/address register or two 8-bit registers
SP - stack pointer, 16 bits
PC - program counter, 16 bits

Registers introduced with the Z80:

IX - 16-bit index or base register for 8-bit immediate offsets
IY - 16-bit index or base register for 8-bit immediate offsets
I - interrupt vector base register, 8 bits
R - DRAM refresh counter, 8 bits (MSB does not count)
AF' - alternate (or shadow) accumulator and flags (*toggled in and out with EX AF,AF'*)
BC',DE', and HL' - alternate (or shadow) registers (*toggled in and out with EXX*)
Four bits of interrupt status and interrupt mode status

3. Microprocessador Z80

Arquitetura Zilog Z80

Interrupt Page Address Register (I)

The Z80 CPU can be operated in a mode where an indirect call to any memory location can be achieved in response to an interrupt. The I register is used for this purpose and stores the high order eight bits of the indirect address while the interrupting device provides the lower eight bits of the address. This feature allows interrupt routines to be dynamically located anywhere in memory with minimal access time to the routine.

Memory Refresh Register (R)

The Z80 CPU contains a memory refresh counter, enabling dynamic memories to be used with the same ease as static memories. Seven bits of this 8 bit register are automatically incremented after each instruction fetch. The eighth bit remains as programmed, resulting from an LD R, A instruction. The data in the refresh counter is sent out on the lower portion of the address bus along with a refresh control signal while the CPU is decoding and executing the fetched instruction. This mode of refresh is transparent to the programmer and does not slow the CPU operation. The programmer can load the R register for testing purposes, but this register is normally not used by the programmer. During refresh, the contents of the I register are placed on the upper eight bits of the address bus.

4. Microprocessador Motorola 68000

Família Motorola 68000

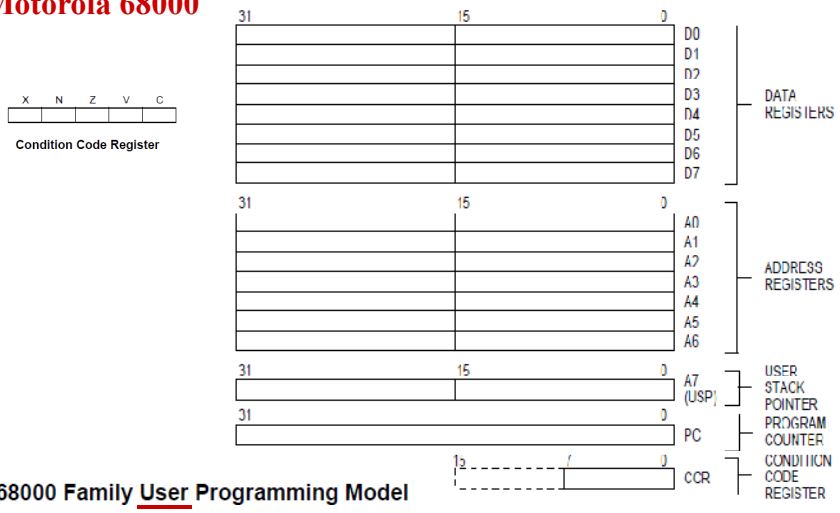
Microprocessors and coprocessors in the M68000 family, including: [1979]

MC68000	—	16-/32-Bit Microprocessor
MC68EC000	—	16-/32-Bit Embedded Controller
MC68HC000	—	Low Power 16-/32-Bit Microprocessor
MC68008	—	16-Bit Microprocessor with 8-Bit Data Bus
MC68010	—	16-/32-Bit Virtual Memory Microprocessor
MC68020	—	32-Bit Virtual Memory Microprocessor
MC68EC020	—	32-Bit Embedded Controller
MC68030	—	Second-Generation 32-Bit Enhanced Microprocessor
MC68EC030	—	32-Bit Embedded Controller
MC68040	—	Third-Generation 32-Bit Microprocessor
MC68LC040	—	Third-Generation 32-Bit Microprocessor
MC68EC040	—	32-Bit Embedded Controller
MC68330	—	Integrated CPU32 Processor
MC68340	—	Integrated Processor with DMA
MC68851	—	Paged Memory Management Unit
MC68881	—	Floating-Point Coprocessor
MC68882	—	Enhanced Floating-Point Coprocessor

4. Microprocessador Motorola 68000

Arquitetura Motorola 68000

16 General-Purpose 32-Bit Registers (D7 – D0, A7 – A0)
32-Bit Program Counter (PC)
8-Bit Condition Code Register (CCR)

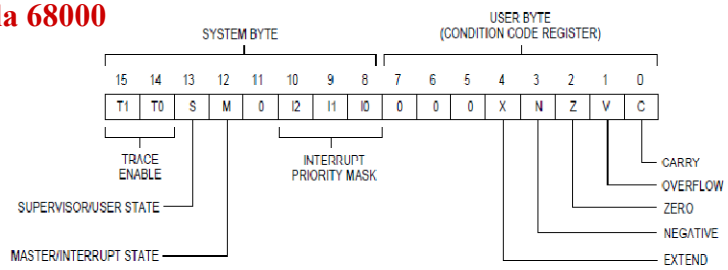


Condition Code Register

M68000 Family User Programming Model

4. Microprocessador Motorola 68000

Arquitetura Motorola 68000



T1	T0	TRACE MODE
0	0	NO TRACE
1	0	TRACE ON ANY INSTRUCTION
0	1	TRACE ON CHANGE OF FLOW
1	1	UNDEFINED

S	M	ACTIVE STACK
0	x	USP
1	0	ISP
1	1	MSP

Status Register

M68000 Family User Programming Model

4. Microprocessador Motorola 68000

Arquitetura Motorola 68000

The M68000 family programming model consists of two register groups: User and Supervisor.

User programs executing in the user mode only use the registers in the user group. System software executing in the supervisor mode can access all registers and uses the control registers in the supervisor group to perform supervisor functions.

System programers use the supervisor programming model to implement sensitive operating system functions—e.g., I/O control and memory management unit (MMU) subsystems. There are registers accessible only in the supervisor programming mode. They can only be accessed via privileged instructions.

SUPERVISOR PROGRAMMING MODEL

4. Microprocessador Motorola 68000

Arquitetura Motorola 68000

SUPERVISOR PROGRAMMING MODEL

AC1, AC0 = Access Control Registers
ACUSR = Access Control Unit Status Register
CAAR = Cache Address Register
CACR = Cache Control Register
DACR1, DACR0 = Data Access ControlRegisters
DFC = Destination Function Code Register
DTT1, DTT0 = Data Transparent Translation Registers
IACR1, IACR0 = Instruction Access Control Registers
ITT1, ITT0 = Instruction Transparent Translation Registers
MSP = Master Stack Pointer Register
SFC = Source Function Code Register
SR = Status Register
SSP/ISP = Supervisor and Interrupt Stack Pointer
TT1, TT0 = Transparent Translation Registers
VBR = Vector Base Register

Registers	Devices			
	68851	68030	68040	68LC040
AC	x			
CAL	x			
CRP	x	x		
DRP	x			
PCSR	x			
PMMUSR, MMUSR	x	x	x	x
SCC	x			
SRP	x	x	x	x
TC	x	x	x	x
URP			x	x
VAL	x			

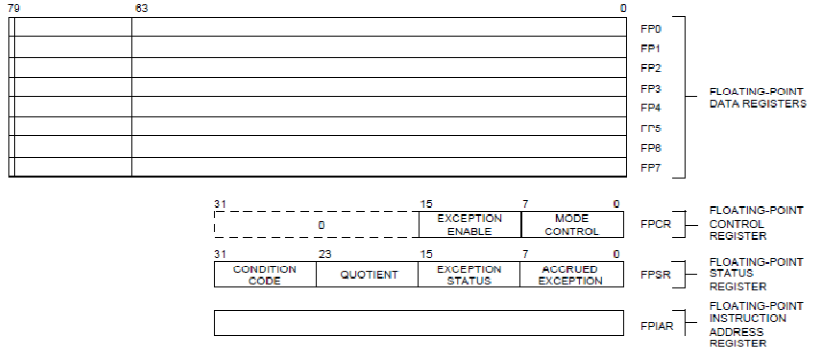
Registers	Devices								
	68000 68008 68HC000 68HC001 68EC000	68010	68020 68EC020	CPU32	68030	68EC030	68040	68EC040	68LC040
AC1, AC0						x			
ACUSR						x			
CAAR			x		x	x			
CACR			x		x	x	x	x	x
DACR1, DACR0								x	
DFC		x	x	x	x	x	x	x	x
DTT1, DTT0							x		x
IACR1, IACR0								x	
ITT1, ITT0							x		x
MSP			x		x	x	x	x	x
SFC		x	x	x	x	x	x	x	x
SR	x	x	x	x	x	x	x	x	x
SSP/ISP	x	x	x	x	x	x	x	x	x
TT1, TT0					x				
VBR		x	x	x	x	x	x	x	x

USP - SSC-510 - Informática T1 / 2009-2
Arquitetura de Computadores
Prof. Fernando Osório

4. Microprocessador Motorola 68000

Arquitetura Motorola 68K FPU

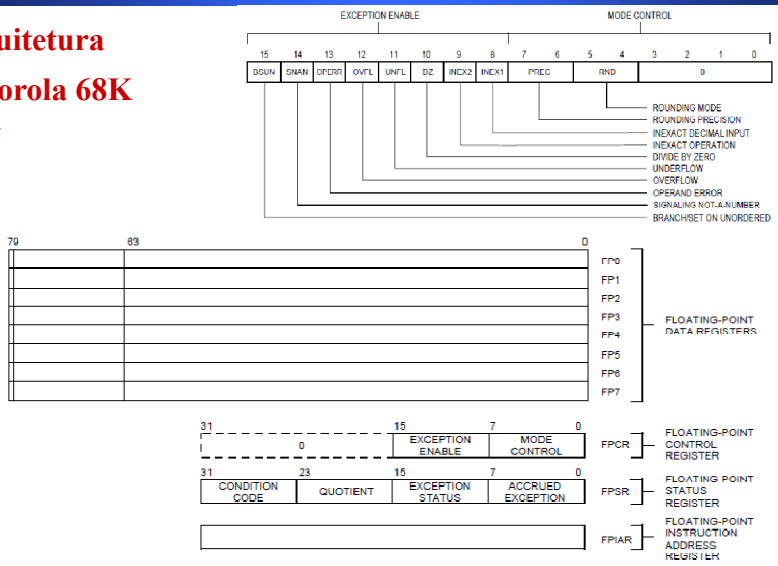
8 Floating-Point Data Registers (FP7 – FP0)
16-Bit Floating-Point Control Register (FPCR)
32-Bit Floating-Point Status Register (FPSR)
32-Bit Floating-Point Instruction Address Register (FPIAR)



M68000 Family Floating-Point Unit User Programming Model

4. Microprocessador Motorola 68000

Arquitetura Motorola 68K FPU

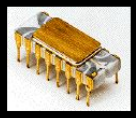


M68000 Family Floating-Point Unit User Programming Model

4. Microprocessador Motorola 68000

Arquiteturas do 4004 ao 68000

Intel 4004



Generally regarded as the very first single-chip microprocessor, the 4004 was designed almost by accident. Intel was contracted to create a custom chip for a desktop calculator — the firm had done three or four of those already — but decided it could do the job more efficiently with a flexible, multi-purpose chip, which could be re-used again and again in different applications. This was the very modest start of a truly great idea. It didn't power any computers as we understand the term today — the microcomputer was not invented yet — just simpler machines.

The tiny 0.74MHz 4-bit 4004 had a short and unspectacular market life, and very little power even by the standards of the day, but it was the forerunner of the more successful 8-bit 8008 and then the first really successful CPU, the Intel 8080.

Form	Design	Manufacture	Introduction	NPU
16-pin DIP	Intel	Intel	November 1971	none
Internal clock	**External clock**	**L1 cache**	**Width**	**Transistor count**
0.74MHz	0.74MHz	none	4-bit	2250

Web: http://www.redhill.net.au/c/c-1.html

4. Microprocessador Motorola 68000

Arquiteturas do 4004 ao 68000

http://en.wikipedia.org/wiki/MOS_Technology_6502

MOS Technologies 6502

The MOS Technology 6502 is an 8-bit microprocessor that was designed by Chuck Peddle and Bill Mensch for MOS Technology in 1975. When it was introduced, it was the least expensive full-featured microprocessor on the market by a considerable margin, costing less than one-sixth the price of competing designs from larger companies such as Motorola and Intel. The 6502 is an 8-bit processor with a 16-bit address bus.

The 6502 was designed primarily by the same engineering team that had designed the Motorola 6800. After resigning from Motorola en masse, the team went looking for another company that would be interested in hosting a design team, and found MOS Technology, then a small chipmaking company whose main product was a single-chip implementation of the popular Pong video game.

Clock: 1Mz (6502) 2Mz (6502A) 3Mhz (6502B)
Pins: 40-pin DIP
Data Bus: 8 bits
Address Bus: 16 bits (64Kb addressable memory)
Manufacturer: MOS Tech – Year: 1975

A MOS 6502 processor in a DIP-40 plastic package.

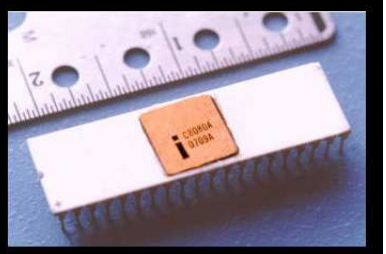
4. Microprocessador Motorola 68000

Arquiteturas do 4004 ao 68000

Intel 8080
Microprocessador de 8/16 bits dados e 16 bits de endereço

The classic Intel CPU. This was the heart of most of the world's first microcomputers, including the Altair 8800. (Pictured in the 8085 entry below.) All modern PCs use descendants of the 8080. Indeed, an Athlon 64 or a Pentium 4 can still run something very like 8080 code!

Despite its huge influence and massive sales, the 8080 was soon overshadowed in the marketplace by the more advanced Zilog Z-80, which built on the 8080's success and owed a lot to it. Introduced at 2MHz, as time went by the 8080 was pushed up to just over 3MHz.



http://www.redhill.net.au/c/c-1.html
http://en.wikipedia.org/wiki/Intel_8080

Clock: 2Mz / 3Mhz
Pins: 40-pin DIP
Data Bus: 8 bits
Address Bus: 16 bits
Manufacturer: Intel – Year: 1974

The processor had seven 8-bit registers, (A, B, C, D, E, H, and L)
Register A: 8-bit accumulator, 16-bit register in pairs (BC, DE, HL)
The address bus had its own 16 pins, and the data bus had 8 pins
(64Kb addressable memory)

4. Microprocessador Motorola 68000

Zilog Z-80

The most successful microprocessor of all time.

Zilog was formed by a group of ex-Intel engineers who set out to improve on the 8080 but still maintain compatibility with it. The Z-80 sold in huge quantities, and was at the heart of most of the microcomputers of the CPM era. Apple and Commodore used the 6502, but nearly all the other successful manufacturers used a Z-80. Programmers loved it for its power and simplicity and Zilog pushed it to faster and faster clock speeds over the years. It was more than a match for the clumsy first-generation 16-bit CPUs like the Intel 8086 and can still do useful work. Incredibly, versions of the 30-year-old 8-bit Z-80 are still in production!

Zilog's follow-up designs, however, were over-ambitious, and the 16 and 32-bit Z-800 and Z-8000 were very late to market and suffered from teething troubles. The Z-80, by the way, introduced the idea of SIMD (Single Instruction, Multiple Data) with its block move and copy instructions. These were considered very powerful at the time: real mainframe stuff. Modern SSE instructions work on highly advanced versions of this same basic principle.

Form	Design	Manufacture	Introduction	NPU
40-pin DIP	Zilog	Zilog	July 1976	external
Internal clock	**External clock**	**L1 cache**	**Width**	**Transistor count**
2.5-12MHz	2.5-12MHz	none	8-bit with 16-bit elements	About 6000

4. Microprocessador Motorola 68000

Motorola 68000 Family

The best of the 16-bit CPUs, though quite expensive.

The 68000 powered almost everything that didn't have an 8086 or 8088: Apple Lisa, Apple Mac, Commodore Amiga, Atari ST, and many others. The simple, practical design lasted well, and was updated with the 68020, 68030 and 68040. Programmers loved the 68000 (no-one ever loved an 8088) and 68000 code tends to be small, fast and efficient. Notice how 68000 powered Amigas and Macs used to do things in 1MB or 2MB of RAM that you needed 16MB and a 486 to do on a PC.

Like the Z-80 and the 386, the 68000 lives on as an embedded processor for industrial automation work.

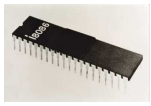
It's not meaningful to give transistor count and clock speed figures here, as there have been numerous variations and developments within the 68000 family — much like the X86 family with its 8086, 286, 386 and so on. The last of them were roughly equivalent to the Pentium. By that time, Apple had switched to the Power PC, and most of the other 68000-based manufacturers had disappeared.

Illustration: a 68020 from the mid to late Eighties.

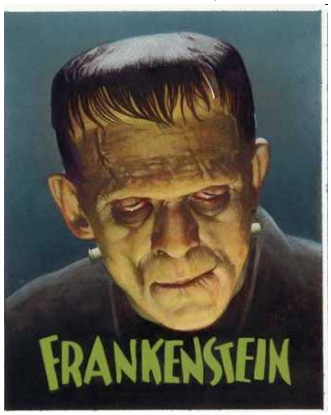
Version	Clock	Introduction	Width	Transistor Count
68000		September 1979	16-bit	68 thousand
68020		June 1984	32-bit	.
68030	50MHz	April 1989	32-bit	.
68040	25MHz	January 1990	32-bit	1.2 million

5. Microprocessador Intel 8086

Arquiteturas do Intel 8086 / 8088



Microprocessador: [1978]
16 bits dados
20 bits de endereço
4,77 MHz



5. Microprocessador Intel 8086

Arquiteturas do Intel 8086 / 8088

Microprocessador: [1978]
8/16 bits dados
20 bits de endereço
4,77 MHz

8086 - primeiro microprocessador de 16 bits da Intel

- Arquitetura de 16 bits
  - Comunicação com a memória em 16 bits (8086)
  - Capacidade máxima de memória de 1 MByte
  - Registradores: 14 regs.
    4 regs. dado, 4 regs. endereço,
    4 regs. segmento, reg. ponteiro do programa, reg. flags
  - Endereço físico = segmento * 16 + deslocamento **(!)**
  - Instruções básicas: 85
  - Co-processador: 8087 (67 instruções básicas)
  - Sem cache, sem memória virtual
- 8088: Mesma arquitetura, barramento externo de 8 bits

5. Microprocessador Intel 8086

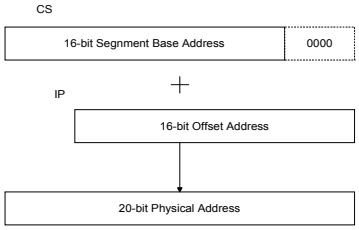
Arquiteturas

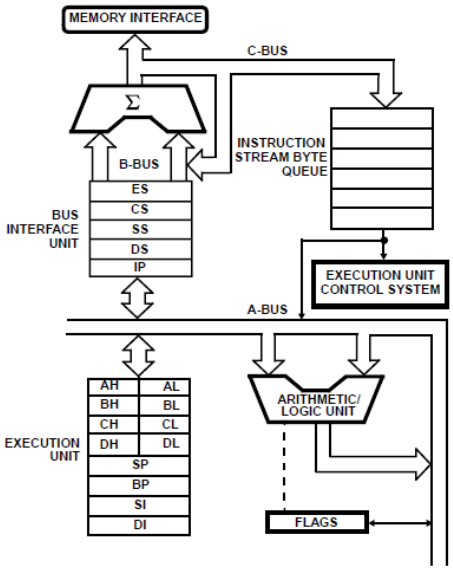
Intel 8086 / 8088

AH, AL: 8 bits
AX: AH + AL = 16 bits

CS: Code Segment = 16 bits
IP : Instruction Pointer = 16 bits

Program Counter: CS + IP
16 bits / 16 bits => 20 bits



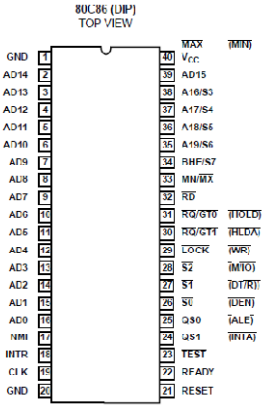


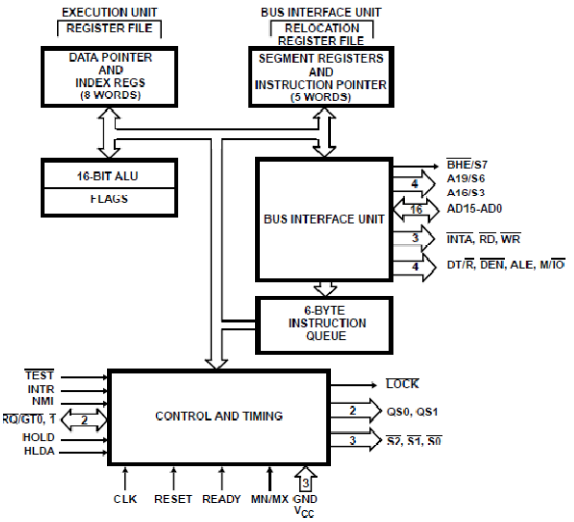
5. Microprocessador Intel 8086

Arquiteturas

Intel 8086 / 8088

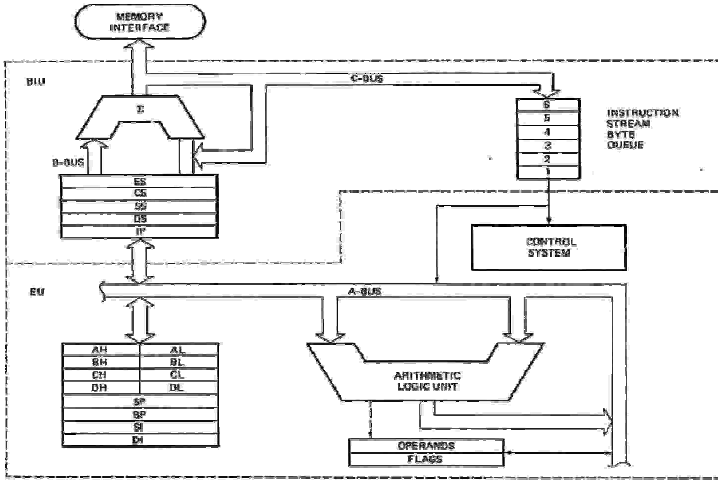
Functional Diagram





5. Microprocessador Intel 8086

Arquiteturas Intel 8086 / 8088



8086 internal block diagram. (*Intel Corp.*)

5. Microprocessador Intel 8086

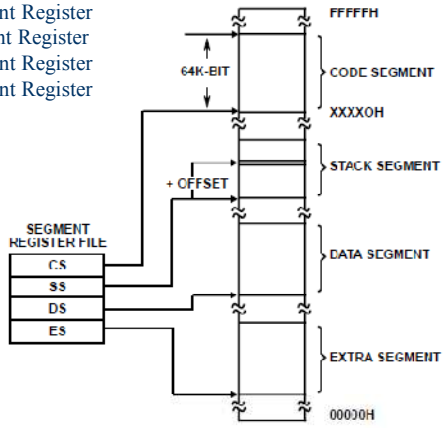
Arquiteturas Intel 8086 / 8088

AX - Accumulator
BX - Base Register
CX - Count Register
DX - Data Register

IP - Instruction Pointer
CS - Code Segment Register
DS - Data Segment Register
SS - Stack Segment Register
ES - Extra Segment Register

SP - Stack Pointer
BP - Base Pointer
SI - Source Index Register
DI - Destination Register

TYPE OF MEMORY REFERENCE	DEFAULT SEGMENT BASE	ALTERNATE SEGMENT BASE	OFFSET
Instruction Fetch	CS	None	IP
Stack Operation	SS	None	SP
Variable (except following)	DS	CS, ES, SS	Effective Address
String Source	DS	CS, ES, SS	SI
String Destination	ES	None	DI
BP Used As Base Register	SS	CS, DS, ES	Effective Address



80C86 MEMORY ORGANIZATION

5. Microprocessador Intel 8086

Arquiteturas Intel 8086 / 8088

AX - Accumulator
BX - Base Register
CX - Count Register
DX - Data Register

SP - Stack Pointer
BP - Base Pointer
SI - Source Index Register
DI - Destination Register

IP - Instruction Pointer
CS - Code Segment Register
DS - Data Segment Register
SS - Stack Segment Register
ES - Extra Segment Register

FLAGs:

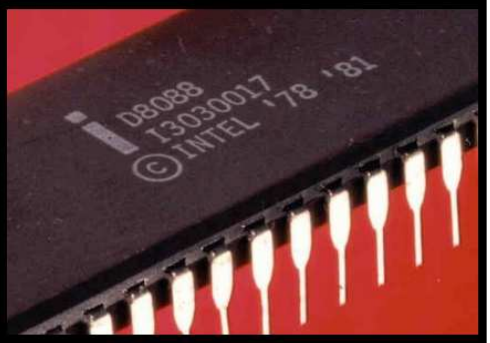
Bit 0 - CF Carry Flag - Set by carry out of msb
Bit 2 - PF Parity Flag - Set if result has even parity
Bit 4 - AF Auxiliary Flag - for BCD arithmetic
Bit 6 - ZF Zero Flag - Set if result is zero
Bit 7 - SF Sign Flag = msb of result
Bit 8 - TF Single Step Trap Flag
Bit 9 - IF Interrupt Enable Flag
Bit 10 - DF String Instruction Direction Flag
Bit 11 - OF Overflow Flag

Bits 1, 3, 5, 12-15 are undefined.

USP - SSC-510 - Informática T1 / 2009-2
Arquitetura de Computadores
Prof. Fernando Osório

5. Microprocessador Intel 8086

Intel 8086 and 8088



The chip that powered the original IBM PC, and thousands of other models too. All later X86 designs (286, 386, 486, Pentium, and so on) have built on this foundation.

There were four main 16-bit CPUs at this time. The Texas Instruments TI 9900 was an early leader but badly marketed. The Zilog Z-800 was powerful but late and buggy. The expensive Motorola 68000 was generally regarded as the best choice with its combination of simplicity and power. But the 8086 family ended up as easily the most successful of them all.

The main reasons were its compatibility with the 8080/8085 and Z-80 family, its relatively low price, and above all, the 8088 variant. The 8088 was a hybrid 8/16-bit design: 16-bit internally, with 8-bit I/O. This meant that system designers could use cheap and readily available 8-bit support chips, and reduce the cost of the system by hundreds of dollars. Performance wasn't outstanding, and the lean, mean Z-80 and 8085 machines were often superior, but the 8088 sold well.

It got its biggest break when a small sub-division of IBM couldn't afford to pay cash for their first choice CPU, the Motorola 68000, and used the 8088 for the IBM PC. This made the 8088 respectable and the rest, as they say, was history. It sold in countless millions and, as an all time success story, is second only to the Z-80. (Those who claim the reverse order are showing their youth.)

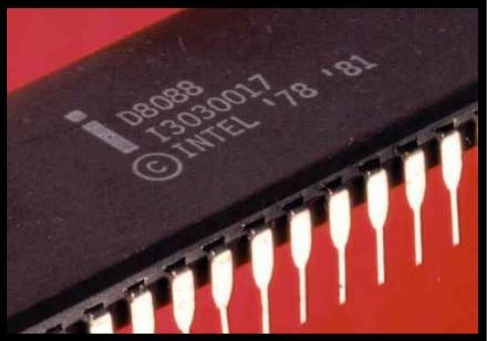
Unfortunately, Intel made some very bad design decisions with this chip. First, it used a segmented architecture (see 286 below). Secondly, for some incomprehensible reason, Intel chose to organise its memory access in such a way that IBM felt constrained to limit the theoretical maximum RAM of the original PC to 640k. Even in those early days, these were short-sighted decisions, and we have all suffered from them ever since. If you've ever had an 'out of memory' error message, then you have met this design fault yourself. DOS, Windows, and even Windows 98 all have base-memory problems which are directly caused by the 640k barrier. Only true 32-bit operating systems like Linux, OS/2 and Windows 2000 escape this problem, and for these we had to wait seven more years for the 386.

5. Microprocessador Intel 8086

Intel 8086 and 8088

The chip that powered the original IBM PC, and thousands of other models too. All later X86 designs (286, 386, 486, Pentium, and so on) have built on this foundation.

There were four main 16-bit CPUs at this time. The Texas Instruments TI 9900 was an early leader but badly marketed. The Zilog Z-800 was powerful but late and buggy. The expensive Motorola 68000 was generally regarded as the best choice with its combination of simplicity and power. But the 8086 family ended up as easily the most successful of them all.



The main reasons were its compatibility with the 8080/8085 and Z-80 family, its relatively low price, and above all, the 8088 variant. The 8088 was a hybrid 8/16-bit design: 16-bit internally, with 8-bit I/O. This meant that system designers could use cheap and readily available 8-bit support chips, and reduce the cost of the system by hundreds of dollars. Performance wasn't outstanding, and the lean, mean Z-80 and 8085 machines were often superior, but the 8088 sold well.

It got its biggest break when a small sub-division of IBM couldn't afford to pay cash for their first choice CPU, the Motorola 68000, and used the 8088 for the IBM PC. This made the 8088 respectable and the rest, as they say, was history. It sold in countless millions and, as an all time success story, is second only to the Z-80. (Those who claim the reverse order are showing their youth.)

Unfortunately, Intel made some very bad design decisions with this chip. First, it used a segmented architecture (see 286 below).

Form	Design	Manufacture	L1 cache	NPU
40-pin DIP	Intel	Intel, AMD, Harris, Siemens, Hitachi	none	8087 or Weitek
Internal clock	External clock	Width	Introduction	Transistor count
5-12MHz	5-12MHz	16-bit (8086)	June 1978	29 thousand
4-12MHz	4-12MHz	8/16-bit hybrid (8088)	June 1979	29 thousand

6. Microprocessadores x86

Família Intel 8086: x86

80186, 80286, 386, 486, 486SX/DX, Pentium (MMX, II, III, Pro, Xeon, P4)
Intel Celeron, Intel Centrino, ...

Do 8086 ao DX4

Chip	ALU	reg	dado	End.	Cache	Características
8088(6)	16	16	8 (16)	20	-	micro de 16 bits
80186	16	16	16	20	-	8086 & circuitos de apoio
80286	16	16	16	24	-	memória virtual segmentada e modo protegido
386SX	32	32	16	32	-	80386 simplificado
80386	32	32	32	32	-	MMU, 32 bits e modo virtual
486SX	32	32	32	32	8K	80486 sem FPU
80486	32	32	32	32	8K	80386 com FPU
486DX2	32	32	32	32	8K	486 com frequência interna de clock dupla
DX4	32	32	32	32	8K instr. 8K dado	486 com frequência interna de clock tripla

* Ref.: Weber, Raul – Inf112 / Livro: Arquitetura de Computadores Pessoais. Bookman, 2008.

Família Intel 8086: x86

Do Pentium ao Pentium II

Chip	ALU	reg	dado	End.	Cache	Características
Pentium	32	32	64	32	8K instr. 8K dado	2 pipelines inteiros, FPU de 64 bits, lógica de previsão de desvios
Pentium Pro	32	32	64	36	8K instr. 8K dado 256Knivel2	Pentium, mais renomeação de registradores e execução fora de sequência
Pentium MMX	32	32	64	32	16K instr. 16K dado	Pentium, com instruções extras para paralelismo (SIMD)
Pentium II	32	32	64	36	16K instr. 16K dado 512Knivel2	Pentium Pro com MMX
Pentium II Celeron	32	32	64	36	16K instr. 16K dado 0K nivel 2	Pentium II sem cache de nivel 2
Pentium II Celeron A	32	32	64	36	16K instr. 16K dado 128Knivel2	Pentium II com cache na mesma frequência da CPU
Pentium II Xeon	32	32	64	36	16K instr. 16K dado cache niv.2	Pentium II com 512K/1M/2M de cache na mesma frequência da CPU

* Ref.: Weber, Raul – Inf112 / Livro: Arquitetura de Computadores Pessoais. Bookman, 2008.

USP - SSC-510 - Informática T1 / 2009-2
Arquitetura de Computadores
Prof. Fernando Osório

6. Microprocessadores x86

Família Intel 8086: x86

Do Pentium III ao Pentium 4

Chip	ALU	reg	dado	end.	Cache	Características
Pentium III	32	32	64	36	16K instr. 16K dado cache niv.2	Pentium II com instruções extras para paralelismo de ponto flutuante
Pentium 4	32	32	64	36	12K instr. 8K dado cache niv.2	Pentium III com instruções extras para paralelismo
Pentium4 HT	32	32	64	36	12K instr 16K dado cache niv.2	Pentium 4 com unidades de execução duplicadas

Pentium e Pentium MMX - P5
Pentium Pro a Pentium 4 - P6

* Ref.: Weber, Raul – Inf112 / Livro: Arquitetura de Computadores Pessoais. Bookman, 2008.

6. Microprocessadores x86

Família Intel 8086: x86

Características tecnológicas

Processador	Cache	tipo	nível 2	frequência	mult.	Tensão	Transistor
8088(6)	-	-	-	-	1x	5 V	29.000
80286	-	-	-	-	1x	5 V	134.000
80386	-	-	-	-	1x	5 V	275.000
486SX	8K	WT	-	-	1x	5 V	1.185.000
486DX	8K	WT	-	-	1x	5 V	1.200.000
486DX2	8K	WT	-	-	2x	5 V	1.100.000
DX4	16K	WT	-	-	2-3x	3,3 V	1.600.000
Pentium 60/66	2x8K	WB	-	-	1x	5 V	3.100.000
Pentium 75/200	2x8K	WB	-	-	1,5-3x	3,3 V	3.300.000
Pentium Pro	2x8K	WB	256K	1	2-3x	3,3 V	5.500.000
Pentium MMX	2x16K	WB	-	-	1,5-3x	1,8-2,8 V	4.100.000
Pentium II	2x16K	WB	512K	1/2	3,5-5x	1,8-2,8 V	7.500.000
Celeron	2x16K	WB	0K	-	3,5-5x	1,8-2,8 V	7.500.000
Celeron A	2x16K	WB	128K	1	3,5-5x	1,8-2,8 V	7.500.000
Xeon	2x16K	WB	512K-2M	1	3,5-5x	1,8-2,8 V	7.500.000
Pentium III	2x16K	WB	512K	1/2	3,5-5x	1,8-2,8 V	9.500.000
Pentium 4	8K	WB	256K	1	3,0-4x	1,3-1,7 V	42.000.000
Pentium 4 HT	16K	WB	1M	1	4-6x	1,3-1,7V	125M

* Ref.: Weber, Raul – Inf112 / Livro: Arquitetura de Computadores Pessoais. Bookman, 2008.

USP - SSC-510 - Informática T1 / 2009-2
Arquitetura de Computadores
Prof. Fernando Osório

6. Microprocessadores x86

Família Intel 8086: x86

Computadores Pessoais tipo PC

Tipos	PC XT	PC AT	PC AT 386	PC AT 486	Pentium P5	Pentium P6
microprocessador	8088	80286	80386	80486	Pentium, MMX	Pentium Pro,II,III, 4
FPU	8087	80287	80387	interna	interna	Interna
barramento de dados	8 bits	16 bits	32 bits	32 bits	64 bits	64 bits
barramento de endereços	20 bits	24 bits	30 bits	30 bits	30 bits	33 bits

computadores pessoais do tipo PC ou IBM-PC:
- atualmente chamados computadores de mesa
- também com microprocessadores de outras famílias
- existem computadores pessoais não compatíveis com IBM-PC

* Ref.: Weber, Raul – Inf112 / Livro: Arquitetura de Computadores Pessoais. Bookman, 2008.

INFORMAÇÕES SOBRE A DISCIPLINA

USP - Universidade de São Paulo - São Carlos, SP
ICMC - Instituto de Ciências Matemáticas e de Computação
SSC - Departamento de Sistemas de Computação

Prof. Fernando Santos OSÓRIO
Web institucional: http://www.icmc.usp.br/ssc/
Página pessoal: http://www.icmc.usp.br/~fosorio/
E-mail: fosorio [at] icmc. usp. br ou fosorio [at] gmail. com

Disciplina de Arquitetura de Computadores / Informática
Estagiário PAE: Maurício A. Dias
Web disciplina: COTEIA - Http://coteia.icmc.usp.br
> Programa, Material de Aulas, Critérios de Avaliação,
> Lista de Exercícios, Trabalhos Práticos, Datas das Provas

Visite regularmente o site da CoTeia - Material em permanente atualização